REMARKS

Applicants acknowledge the allowance of Claims 26-28, as well as the indication of the allowability of the subject matter of Claims 16-25, as set forth in paragraphs 5 and 6 on page 4 of the Office Action. In particular, Claims 16-25 would be allowable if rewritten in independent form. Accordingly, in view of the foregoing amendment in which Claim 16 has been rewritten in independent form; and for the reasons set forth hereinafter with regard to independent Claims 15 and 29 as well, Applicants respectfully submit that Claims 16-25 are now allowable.

Claims 15 and 29 have been rejected under 35 U.S.C. § 102(b) as anticipated by Whitehouse et al (U.S. Patent No. 5,872,934). However, as discussed in more detail hereinbelow, Applicants respectfully submit that Claims 15 and 29 distinguish over the Whitehouse et al reference, whether considered by itself, or in combination with other references.

The present invention is directed to a method and apparatus for automatically assigning addresses to a plurality of control units which are connected to a bus system, such as is commonly found in a vehicle. In such networks, the respective control units regularly exchange data via the local

network using assigned addresses, and simultaneously access the data bus for this purpose.

In the address allocation method according to the invention, one of the control units acts as a master unit, transmitting a message to the remaining control units, initiating an address allocation period, during which the remaining control units act as slave units. In response to the message, during the address allocation period, each of the slave units opens a switch contained therein, thereby effectively breaking the data bus line within each slave unit, and causing a dominant signal to be present at its input, which is connected to an output of a preceding slave unit. Each slave unit then detects whether a dominant signal is present at its output (being the input to the next successive slave unit). During a particular cycle of the address allocation period, only that slave unit which does not detect a dominant signal at its output accepts an address transmitted from the master unit, at a preset time during a particular address allocation period.

As best seen in Figure 1, in order to implement the address allocation method according to the invention, each of the respective control units 3, 4, 5, 6 includes an internal switch 9, by which it can interrupt the data line 2, as it passes through, and also a transceiver unit 10 which, when turned on, can send and receive data via the data line 2. In a so-called "dominant state", the transceiver 10 couples the data line 2 to ground 7, such that the data line itself is

at ground level, while in a "recessive state", the transceiver unit effectively disconnects the data line 2 from ground, so that the data line 2 assumes the supply voltage V_{bat}.

Initially, when the address allocation process is commenced, one of the control units, acting as the master control unit (for example, control unit 3) sends a message to the remaining control units, containing an address which is to be allocated. In response to this message, each of the remaining control units 4, 5, 6 opens its switch 9, and sets it transceiver 10 to a state in which it is ready to receive data. Thereafter, commencing with the slave unit 4, which is closest to the master control unit 3, each of the respective control units 4, 5, and 6 determines whether or not the transceiver for the next consecutive (downstream) control unit is in the dominant state, meaning that there exists downstream a control unit which is to be addressed. In this case, the first control unit (for example, control unit 4) closes its switch 9 and turns off its transceiver 10. As a result, the message transmitted on the data line 2 is forwarded to the next respective control unit (5, in the example) which repeats the same process. In the example, if the control unit 6 has not yet been allocated an address, the control unit 5 also closes its switch 9, and turns off its transceiver, so that the message is then forwarded to the control unit 6. However, since there is no control unit downstream from control unit 6, it will not detect the presence of a

downstream transceiver in the dominant state, and therefore its switch 9 remains open and its transceiver 10 remains in a state in which it can receive data. Accordingly, the control unit 6 thereby accepts the address contained in the message from the master control unit 3, and the process is repeated. In the next cycle, control unit 5 is allocated an address, followed by control unit 4 in the next cycle.

Claim 15, as amended, recites that the address allocation period is started by transmitting a message on the common data bus line to the control devices that are to be addressed, such message containing an address that is to be allocated. In addition, Claim 15 also recites that each of the control devices determines "whether there is a downstream control device which is to be addressed" and that "only a control device which determines that there is no downstream control device that is to be addressed accept[s] said address contained in said message".

Similarly, Claim 29 recites that in response to the message, during the address allocation period, each of the slave units opens a switch to break the data bus line within the slave unit, and causes a dominant signal to be present at its input, which is connected to an output of the preceding slave unit. In addition, Claim 29 recites that each slave unit detects whether a dominant signal is present at its output (being, of course, the input of the next succeeding

slave unit). Finally, Claim 29 recites that, "only a slave unit which does not detect a dominant signal at its output accept[s] an address transmitted from the master unit at a preset time during a particular address allocation period".

The latter features of Claims 15 and 29 are not taught or suggested in the Whitehouse et al reference. In fact, Whitehouse et al operates in a manner which is essentially the opposite of the present invention. That is, the respective Smart Video Distribution Units (SVDU's) are programmed sequentially, starting with the upstream SVDU, and each subsequent SVDU is programmed sequentially, at the completion of the programming of the previous upstream SVDU. The procedure by which this is accomplished is described in the specification at Column 4, lines 34-67. In particular, the system control unit SCU transmits a status request on the RS-485 serial data bus, which is received only by the first SVDU 200_1, because the remaining SVDU's are segregated due to the open DPDT relays. Accordingly, the SVDU 200_1 is initially assigned a new address in step 116, and is reconfigured as necessary in step 118. Once this process is completed, the SCU commands the SVDU to close its DPDT relay in step 122, and the process then is repeated.

As can be seen from the foregoing brief description, in Whitehouse et al, there is no disclosure which suggests that the initial message by which an address allocation period is commenced itself contains an address that is to be

allocated, as recited in Claim 15. Moreover, there is also no disclosure that each of the control devices itself determines whether there is a control device downstream of the control device to be addressed, or, more to the point, there is no disclosure that only a control device which determines that there is no downstream control device which is to be addressed accepts the address contained in the initial message by which the address allocation period was commenced. As a result of this arrangement, as defined in Claim 15, the first control device to which a new address is allocated is the last control device contained in the downstream direction, for which there exists no subsequent control device in the downstream direction which remains to have an address allocated to it.

Claim 29 is similarly limited, reciting, as noted previously, that each slave unit detects "whether a dominant signal is present at its output", and that "only a slave unit which does not detect a dominant signal at its output accept[s] an address transmitted from the master unit...".

With regard to the latter feature of the invention, item 4 on page 3 of the Office Action indicates that Whitehouse et al discloses a system in which only a slave unit which does not detect a dominant signal at its output accepts an address transmitted from the master unit, referring in particular to Column 4, lines 42-49. However, Applicants respectfully submit that this portion of the

specification does not disclose such a system. In particular, at Column 4, lines 46-51, the text indicates that, after the SCU transmits a "status request", if a first SVDU responds to the SCU, the SCU then transmits an "assigned new address" command to that SVDU, specifying a new system-unique individual address for that unit. The assignment of such an address, and its acceptance by the particular SVDU in question is therefore unrelated to the condition of any downstream SVDU, or whether the latter has a dominant signal present at its input (connected to the output of the SVDU in question), as recited in Claim 29. Moreover, in Whitehouse et al, the assignment of the new address is contingent only upon the receipt by the SCU of a response from the SVDU in question. Accordingly, Applicants respectfully submit that Whitehouse et al does not teach or suggest a system which includes the steps provided in at least the last two paragraphs of Claim 29.

In light of the foregoing remarks, this application should be in condition for allowance, and early passage of this case to issue is respectfully requested. If there are any questions regarding this amendment or the application in general, a telephone call to the undersigned would be appreciated since this should expedite the prosecution of the application for all concerned.

If necessary to effect a timely response, this paper should be considered as a petition for an Extension of Time sufficient to effect a timely response, and

please charge any deficiency in fees or credit any overpayments to Deposit Account No. 05-1323 (Docket #095309.56351US).

Respectfully submitted,

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